WHAT IS CLAIMED IS:

1. An electrostatic discharge (ESD) protection device, comprising:

a semiconductor bulk of a first conductivity type;

a first doped region of a second conductivity type formed in said semiconductor bulk;

a second doped region of a second conductivity type formed in said semiconductor bulk;

a channel region formed between said first doped region and said second doped region;

a first gate segment formed over a first part of said channel region;

a first field-oxide segment formed over a third part of said channel region; wherein

a first part of said first gate segment overlaps said first field-oxide segment.

2. A device according to Claim 1, wherein said first part is a first end.

3. A device according to Claim 1, wherein said first and third parts form a first continuous portion of said channel.

4. A device according to claim 1, wherein said first gate segment and said first field-oxide segment are substantially collinear.

5. A device according to claim 1, wherein said first gate segment comprises a polysilicon element over an oxide layer.

6. A device according to claim 1, further comprising a plurality of islands formed over said bulk and being enclosed by said first doped region.

7. A device according to claim 6, wherein said plurality of islands comprises a first and second arrays of islands; said first array of islands comprises polysilicon-over-oxide islands; and said second array of

islands comprises field-oxide islands.

8. A device according to claim 7, wherein said first array of islands is closer to said channel region than said second array of islands.

9. A device according to claim 1, further comprising a second gate segment formed over a second part of said channel region; and a first part of said second gate segment overlaps said first field-oxide segment.

10. A device according to Claim 9, wherein said first part of said second gate segment is a first end of said second gate segment.

11. A device according to claim 1, wherein said second and third parts form a second continuous portion of said channel.

12. A device according to claim 1, wherein said first doped region couples to a pad.

13. A device according to claim 1, wherein said second doped region couples to a power bus.

14. An electrostatic discharge (ESD) protection device, comprising:

a semiconductor bulk of a first conductivity type;

a first doped region of a second conductivity type formed in said semiconductor bulk;

a second doped region of a second conductivity type formed in said semiconductor bulk;

a channel region formed between said first and said second doped regions;

said channel region comprising a split-channel region and a non-split-channel region;

said split-channel region including a first and a second sub-channel regions spaced apart from each other; wherein said first sub-channel region being adjacent to said first doped region and said second sub-

channel region being adjacent to said second doped region;

a first gate segment formed over said first sub-channel region;

a second gate segment formed over said second sub-channel region;

a first field-oxide segment formed over said non-split-channel region; and said first and said second gate segments form a stack-gate structure.

15. A device according to claim 14, wherein said first and said second gate segments are substantially parallel to each other.

16. A device according to claim 14, wherein said first gate segment, said second gate segment and said first field-oxide segment are substantially parallel to each other.

17. A device according to claim 14, wherein said split channel region is connected to said non-split channel region to form a continuous channel region.

18. A device according to claim 14, wherein said first gate segment comprises a polysilicon element over an oxide layer.

19. A device according to claim 14, wherein said second gate segment comprises a polysilicon element over an oxide layer.

20. A device according to claim 14, wherein said first gate segment have a first part overlapping a field-oxide extension segment; and said second gate segment have a second part overlapping said field-oxide extension segment.

21. A device according to Claim 20, wherein said first part is a first end; and said second part is a second end.

22. A device according to claim 14, further comprising a plurality of islands formed over said bulk and being enclosed by said first doped region.

23. A device according to claim 22, wherein said plurality of islands comprises a plurality arrays of islands.

24. A device according to claim 14, wherein said first doped region coupling to a pad.

25. A device according to claim 14, wherein said second doped region coupling to a power bus.

26. An electrostatic discharge (ESD) protection device, comprising:

a semiconductor bulk of a first conductivity type;

a first doped region of a second conductivity type formed in said semiconductor bulk;

a second doped region of a second conductivity type formed in said semiconductor bulk;

a channel region formed between said first and said second doped regions;

a first and a second arrays of islands formed over said bulk and being enclosed by said first doped region; wherein

said first array of islands comprising polysilicon-over-oxide islands;

said second array of islands comprising field-oxide islands; and

said first array of islands being closer to said channel region than said second array of islands.